**CMOS VLSI DESIGN**

**LOVELY PROFESSIONAL UNIVERSITY**

**A Project report**

**On**

**Design of an Instrumentation Amplifier in 90 nm CMOS Technology using Cadence Virtuoso**

Submitted in partial fulfillment of the requirements for the award of degree of

**Bachelor of Technology**

**(Electrical and Electronics Engineering)**

**Submitted to**

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### ABSTRACT

Instrumentation amplifiers (INAs) are pivotal components in electronic circuits, renowned for their ability to precisely amplify small differential signals while rejecting noise. Designed for applications requiring accurate signal amplification, INAs boast essential features like high common-mode rejection ratio (CMRR), low noise levels, and precise gain control[1]. They operate with high input impedance and offer excellent temperature stability, making them indispensable in applications ranging from biomedical instrumentation to industrial signal processing. The circuit design of an instrumentation amplifier plays a critical role in achieving high performance, ensuring low DC offset, minimal drift, and robust AC signal analysis. This project focuses on the analysis, design, and implementation of an instrumentation amplifier, emphasizing its core capabilities in differential signal amplification and noise rejection[3].

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**CHAPTER 1 Introduction**

Instrumentation amplifiers (INAs) have emerged as crucial elements in modern electronic circuits due to their unique ability to amplify small differential signals with exceptional precision. A cornerstone of differential amplifier designs, INAs are engineered to amplify the voltage difference between two input signals while minimizing the influence of any common-mode signals. This makes them invaluable in scenarios where accurate signal processing is paramount, such as biomedical signal monitoring, sensor interfacing, and industrial automation[1].

One of the standout attributes of instrumentation amplifiers is their high common-mode rejection ratio (CMRR), which allows them to effectively suppress unwanted noise and common-mode interference. This is particularly critical in environments with significant electrical noise, where the integrity of the desired signal must be preserved[3]. Additionally, INAs exhibit high input impedance, ensuring minimal loading on the signal source, and offer precise gain control, enabling accurate signal amplification over a wide range of input levels.

The design of an instrumentation amplifier also prioritizes low DC offset and minimal drift, characteristics that are essential for maintaining signal fidelity in long-term applications and [2]varying temperature conditions. These features, coupled with a wide frequency range, make INAs suitable for both DC and AC signal analysis. Furthermore, their inherent temperature stability ensures reliable performance across a range of operating environments.

This project delves into the design and simulation of an instrumentation amplifier circuit, exploring its theoretical underpinnings and practical implementation. The circuit aims to exemplify the core principles of INA functionality, including differential signal amplification, noise rejection, and gain precision. Through a detailed analysis of the circuit’s performance, this work highlights the versatility and importance of instrumentation[3] amplifiers in modern electronic applications.

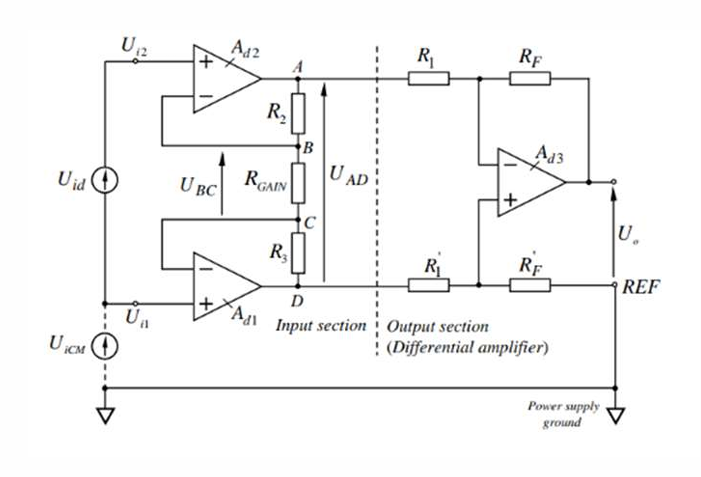


fig: Design method for Instrumentation Amplifier

**CHAPTER 2 PROPOSED DESIGN**

We first designed an operational amplifier (op-amp) sub-circuit using MOS then used three similar op amps along with resistor, capacitor and power source to design an instrumentation amplifier circuit which would meet these specifications shown in the table[3].

|  |  |  |
| --- | --- | --- |
| **PARAMETERS** | **RANGE** | **UNITS** |
| Supply Voltage | 1 | volts |
| Output Range | 2.512 | mv |
| Input Bias Current | 20 | uA |
| Bandwidth | 325 | kHz |
| Supply Current | 20 | uA |
| Gain | 8.001 | db |

**1.Input Stage (Op-Amp 1 and Op-Amp 2):**

* The circuit begins with two identical op-amps in a non-inverting configuration (Op-Amp 1 and Op-Amp 2).
* Each op-amp is connected to one of the input signals, Vin1V\_{in1}Vin1​ and Vin2V\_{in2}Vin2​.
* These op-amps provide high input impedance, ensuring minimal loading on the signal source, making the INA suitable for sensors or weak signal sources.
* A gain resistor RgainR\_{gain}Rgain​ is placed between the two op-amps, controlling the overall gain of the instrumentation amplifier.
* The voltage difference across RgainR\_{gain}Rgain​ determines the differential signal, which is amplified by this stage.

**Gain Expression:**

G=Vout/Vin

20loga(Vout/Vin)

Here, RRR is the feedback resistor for both input op-amps.

**2.Intermediate Stage (Voltage Difference Extraction):**

* The outputs of the two input op-amps are fed into the differential amplifier (Op-Amp) in the second stage.
* This stage amplifies the difference between the two signals: Vout=G⋅(Vin2−Vin1)V\_{out} = G \cdot (V\_{in2} - V\_{in1})Vout​=G⋅(Vin2​−Vin1​)
* The use of precise resistors in this stage ensures accurate differential amplification, while rejecting any common-mode signals (signals present equally on Vin1V\_{in1}Vin1​ and Vin2V\_{in2}Vin2​).

**CHAPTER 3 LADDER LOGIC OF DIFFERENT CIRCUITS**

**3.1:Logic diagram of Instrumentation Amplifier**

1.logic diagram

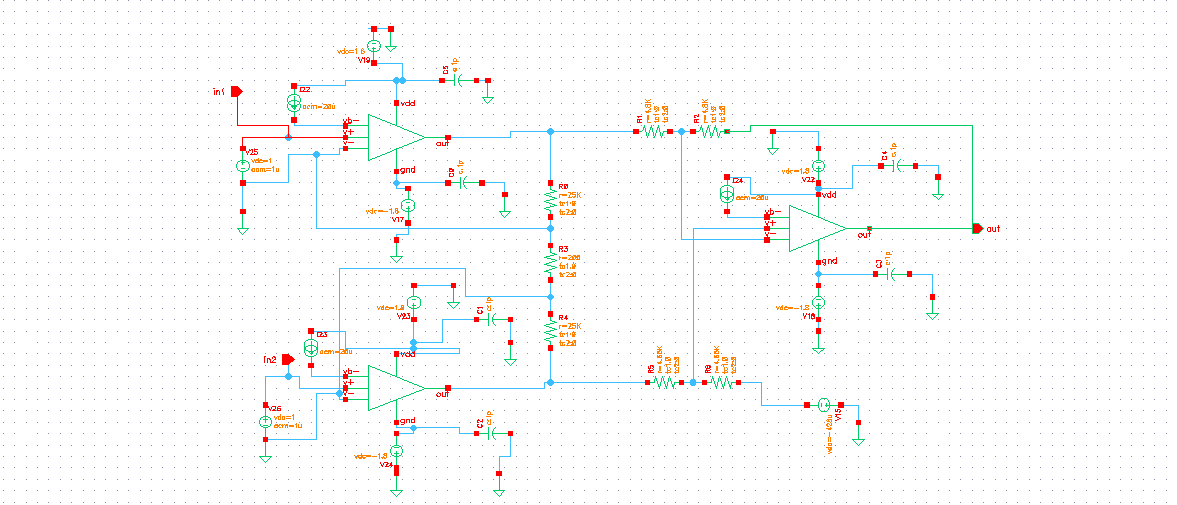


fig1: Instrumentation Amplifierby using 90nm CMOS

**3.2: Operational Amplifier**

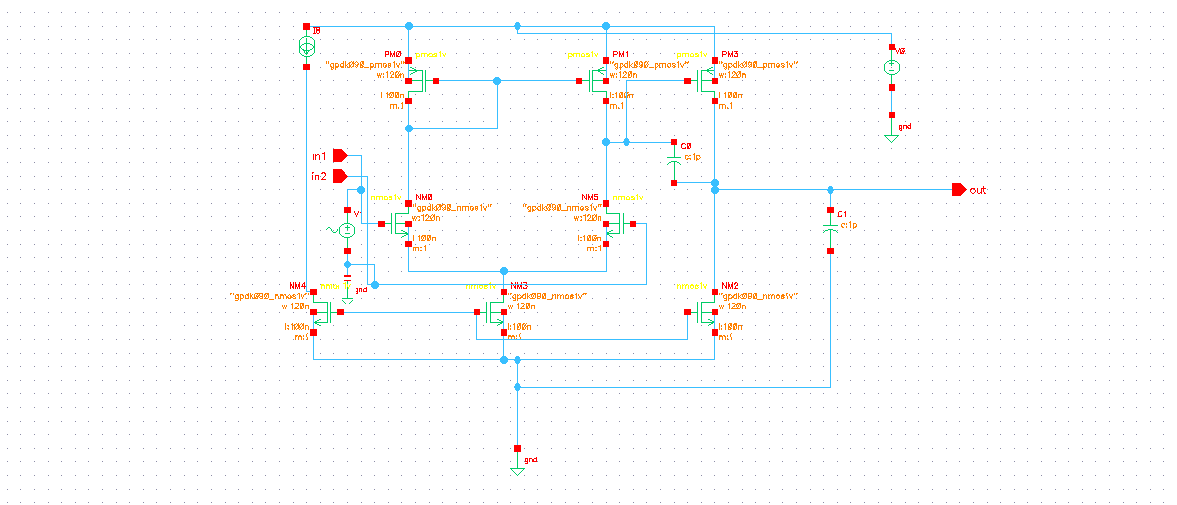
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Fig2: Operational Amplifierby using 90nm CMOS

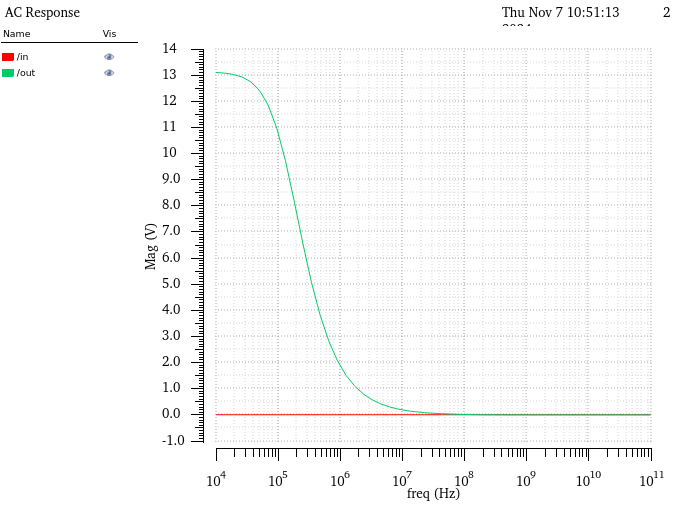
Simulation Result For Operational Amplifier**:**

fig3: AC Response of OP- AMP

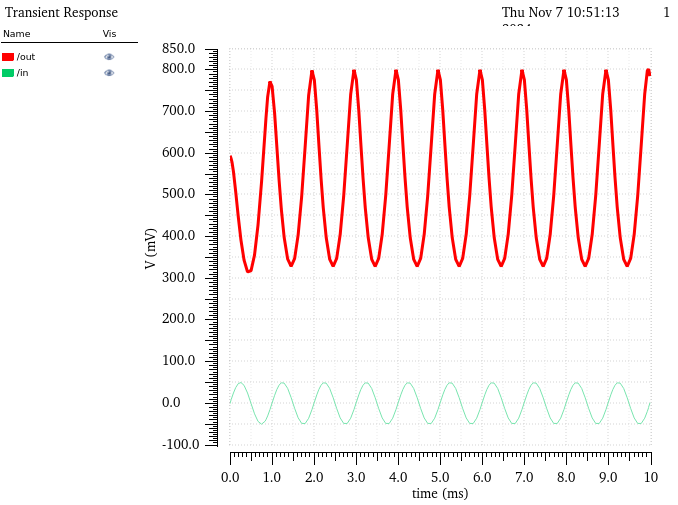
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fig4: Transient Response of OP- AMP

**CHAPTER 4 RESULT ANALYSIS**

**4.1 Corner** **Analysis**

Average Power for Instrumentation AmplifierCalculations:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Analysis** | **NN** | **SS** | **SF** | **FF** |
| Avg Power | 378.7E-6 | 378.63E-6 | 378.41E-6 | 379.82E-6 |

Average Power for OP-AMP

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Analysis** | **NN** | **SS** | **SF** | **FF** |
| Avg Power | 40.27E-9 | 12.97E-9 | 22.64E-9 | 225.9E-9 |

**4.2 Simulation Result**

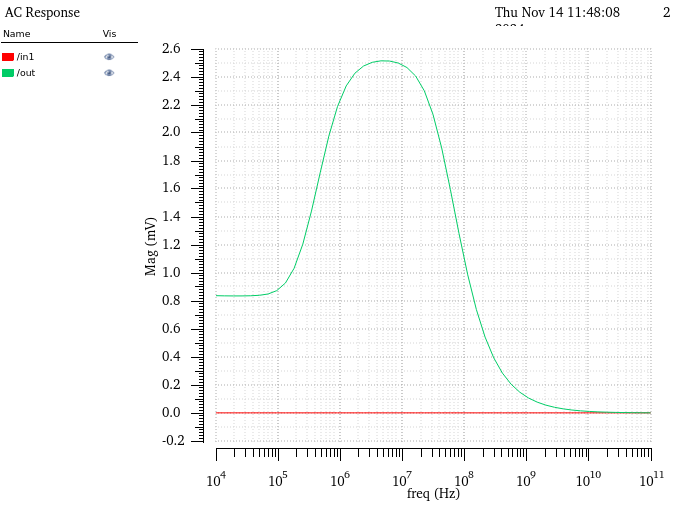
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fig5: AC Response of Instrumentation Amplifier

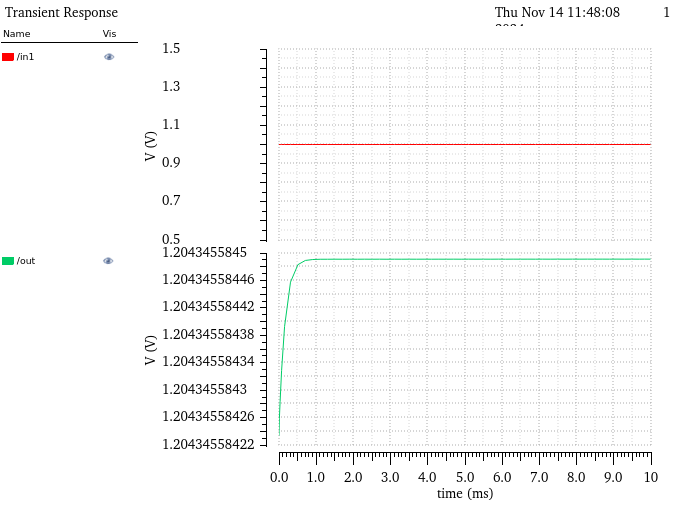
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fig7: Transient Response of Instrumentation Amplifier

**CHAPTER 4 CONCLUSION**

The design and implementation of the instrumentation amplifier using 90 nm CMOS technology in Cadence Virtuoso successfully demonstrate the amplifier's ability to process small differential signals with high precision and noise rejection. This project highlights the fundamental aspects of instrumentation amplifiers, including high common-mode rejection ratio (CMRR), low noise, and precise gain control, making it a robust solution for modern applications requiring accurate signal amplification.

The circuit's architecture, employing two identical operational amplifiers in the input stage and a differential amplifier in the intermediate stage, ensures effective amplification of differential signals while minimizing the influence of common-mode interference. Additionally, the use of precise resistors and symmetrical design enhances the accuracy and stability of the circuit. The corner analysis and simulation results confirm that the designed instrumentation amplifier meets key performance metrics such as high input impedance, minimal power consumption, and wide bandwidth.

This work underscores the importance of CMOS technology in achieving compact, energy-efficient designs while maintaining high performance. The successful implementation of this amplifier paves the way for its application in various fields, such as biomedical instrumentation, sensor interfacing, and industrial automation, where precision signal processing is crucial.

**REFERENCE**

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* Yen CJ, Chung WY, Chi MC. Micro-power low-offset instrumentation amplifier IC design for biomedical system applications. IEEE Transactions on Circuits and Systems I: Regular Papers. 2004 Apr 13;51(4):691-9.
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